

DOT MATRIX LIQUID CRYSTAL DISPLAY MODULE

G12832B-GB Serial

USER' MANUAL

1			

PROPOSED BY		APPROVED
Design	Approved	

深圳市科飞研科技有限公司

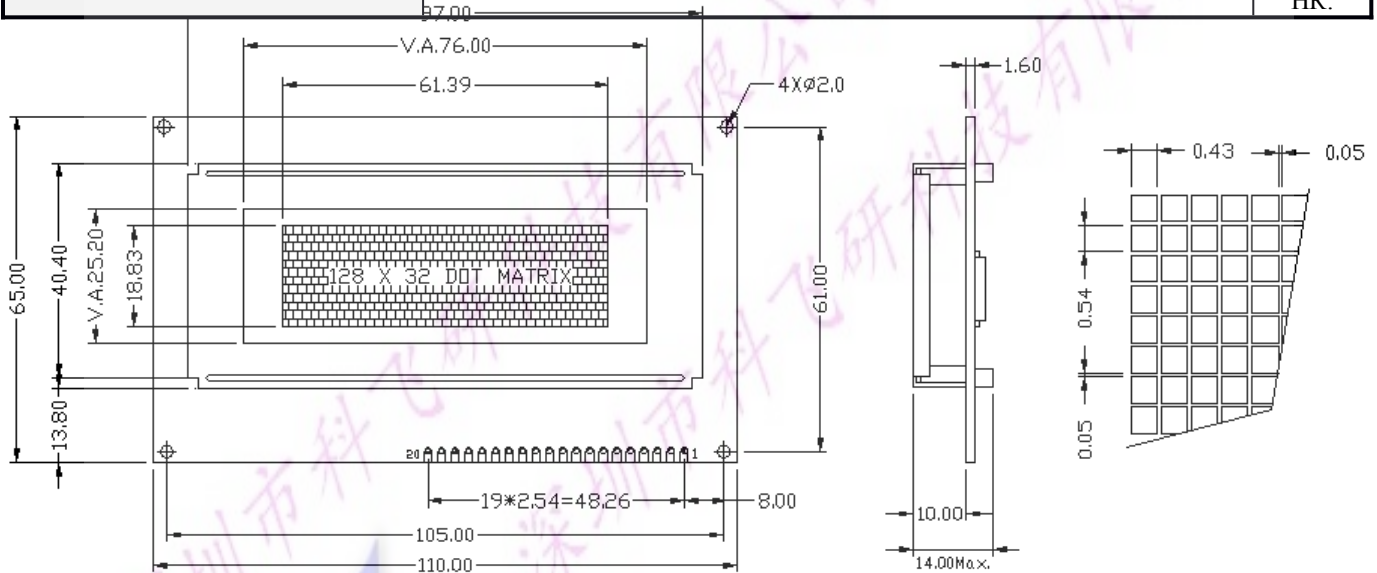


CONTENTS

- 1. Mechanical Specification**
- 2 Mechanical Diagram**
- 3. Interface Pin Connections**
- 4. Absolute Maximum Rating**
- 5. Electrical Characteristics**
- 6. Optical Characteristics**
- 7. Optical Definitions**
- 8. Display Address**
- 9. Interface to MPU**
 - 9.1 Interface to Z-80 CPU
 - 9.2 Interface to MC6800 CPU
 - 9.3 Interface to 4-bit CPU (HMCS43C)
 - 9.4 Interface to HD6805 MP
- 10. Timing Control**
 - 10.1 Write and Read Operation
 - 10.2 Busy flag check timing
- 11. Initialization of LCM**
- 12. Instruction Set**
- 13. User Font Patterns**
- 14. Icon RAM Data**
- 15. Graph Display RAM Address**
- 16. Software Example**
 - 16.1 8-bit operation (8 bits 2 lines)
 - 16.2 4-bit operation (4 bits 2 lines)
- 17. Reliability Condition**
- 18. Function Test & Inspection Criteria**
- 19 Character Generator ROM Map**

1. Mechanical Specification

ITEM	STANDARD VALUE			UNIT
NUMBER OF CHARACTERS	7 CHARACTERS X 2 LINES (16*16 Chinese Font)			--
CHARACTER FORMAT	16 X 16 DOTS			--
MODULE DIMENSION	84.0 (W) X 44.0 (H) X 9.0 (T)	84.0 (W) X 44.0 (H) X 13.20(T)		mm
VIEWING DISPLAY AREA	60.5 (W) X 18.0 (H)			mm
ACTIVE DISPLAY AREA	48.76(W) X 15.32 (H)			mm
DOT SIZE	0.36 (W) X 0.41 (H)			mm
DOT PITCH	0.4 (W) X 0.425(H)			mm
	STN , Yellow Green , 1/32 Duty , 6 O'clock			
	STN , Gray , 1/32 Duty , 6 O'clock , LED Backlight			
	STN , Yellow Green , 1/32 Duty , 6 O'clock , LED Backlight			
	STN , Gray , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
	STN , Yellow Green , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
LED Backlight Color	Yellow Green			
LED Backlight Input	DC +5V	V	100	mA
Backlight Half-Lift Time	50,000			HR.
		V		mA
	37.00			HR.



3. Interface Pin Connections

NO	SYMBOL	LEVEL	FUNCTION	NO	SYMBOL	LEVEL	FUNCTION
1	VSS	--	GND (0V)	11	DB4	H/L	Data Bit 4
2	VDD	H/L	DC +5V	12	DB5	H/L	Data Bit 5
3	VO(NC)	H/L	Contrast Adjust	13	DB6	H/L	Data Bit 6
4	RS(CS)	H/L	Register select	14	DB7	H/L	Data Bit 7
5	R/W(SID)	H/L	Read/Write	15	PSB	H/L	H: Parallel mode L :Serial mode
6	E(CLK)	H,H→L	Enable signal	16	NC	NC	NC
7	DB0	H/L	Data Bit 0	17	/REST	L	Reset signal,active low
8	DB1	H/L	Data Bit 1	18	Vout	+10V	LCD voltage doubler output
9	DB2	H/L	Data Bit 2	19	A(+)	DC +5V	LED Backlight +
10	DB3	H/L	Data Bit 3	20	K(-)	0V	LED Backlight -

4. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYPE	MAX.	UNIT
OPERATING TEMPERATURE	TOP	-20	--	+70	°C
STORAGE TEMPERATURE	TST	-30	--	+80	°C
INPUT VOLTAGE	VI	VSS	--	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	3.0	5.0	6.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	--	--	6.5	V
STATIC ELECTRICITY	Be sure that you are grounded when handing LCM.				

5. Electrical Characteristics

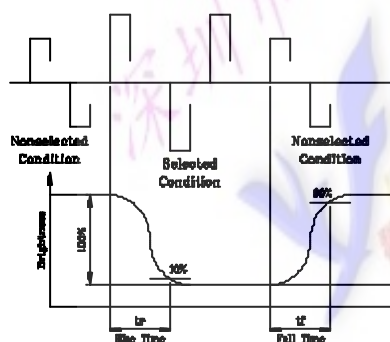
ITEM	SYN	CONDITION	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	3.0	5.0	6.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	Ta= 0 °C	--	6.1	--	V
		Ta= +25 °C	--	5.8	--	V
		Ta= +50 °C	--	5.5	--	V
INPUT HIGH VOLTAGE	VIH	--	2.2	--	VDD	V
INPUT LOW VOLTAGE	VIL	--	0	--	0.6	V
OUTPUT HIGH VOLTAGE	VOH	--	2.4	--	--	V
OUTPUT LOW VOLTAGE	VOL	--	--	--	0.4	V
SUPPLY CURRENT	IDD	VDD=+5V	--	3.0	4.5	mA

6. Optical Characteristics

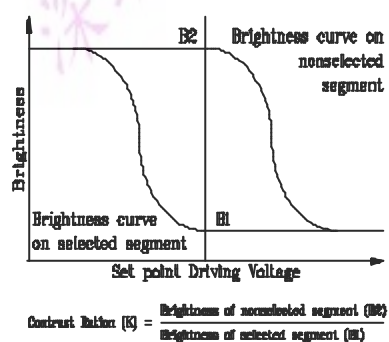
ITEM	SYM	CONDITION	MIN.	TYPE	MAX.	UNIT
VIEW ANGLE (V)	θ	CR ≥ 2	-10	--	40	deg.
VIEW ANGLE (H)	φ	CR ≥ 2	-30	--	30	deg.
CONTRAST RATIO	CR	--	--	5	--	--
RESPONSE TIME	TON	--	--	180	230	mS
RESPONSE TIME	TOFF	--	--	100	150	mS

7. Optical Definitions

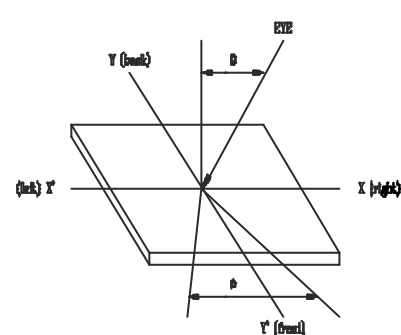
Response Time



Contrast Ration



View Angle



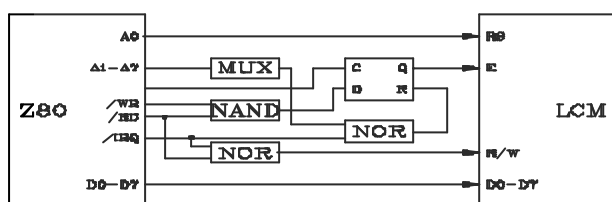
8. Display Address

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80H		81H		82H		83H		84H		85H		86H		87H	
Line 2	90H		91H		92H		93H		94H		95H		96H		97H	
Line 3																
Line 4																

***A Ram Bank is 16-bits (2 bytes)**

9. Interface to MPU

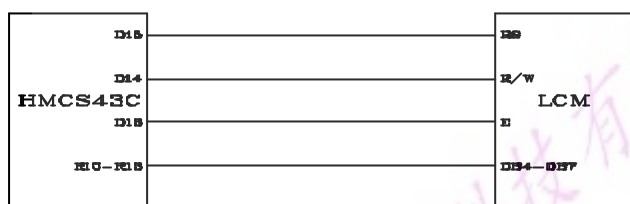
9.1 Interface to Z80 CPU



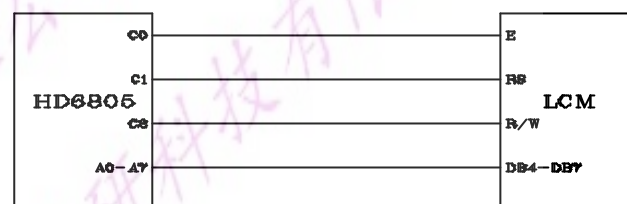
9.2 Interface to MC6800 CPU



9.3 Interface to 4-bit CPU (HMCS43C)



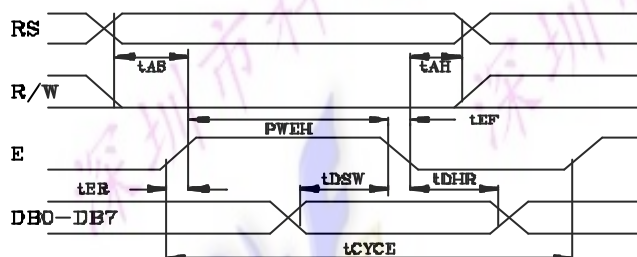
9.4 Interface to HD6805 MP



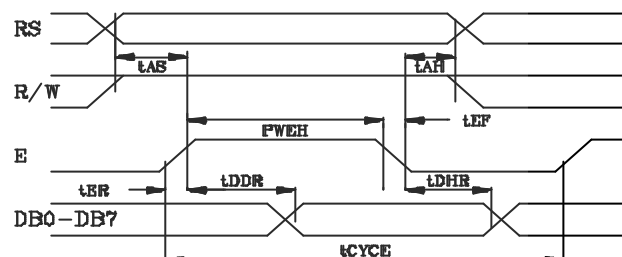
10. Timing Control

10.1 Write and Read Operation

Write Operation

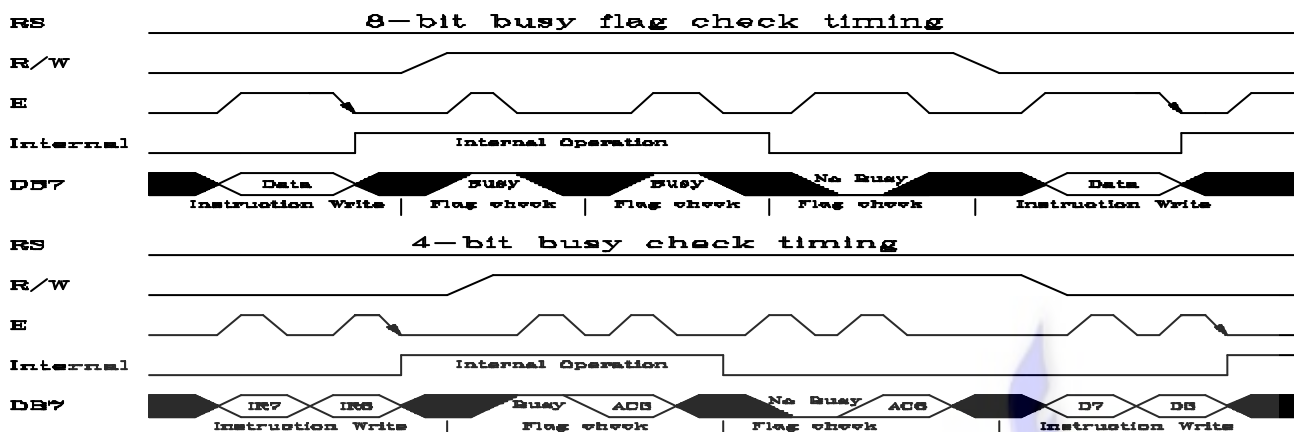


Read Operation



Item	Symbol	Limit (Min.)	Limit (Max.)	Unit
Enable Cycle Time	tCYCE	1200	--	ns
Enable Pules Width (High level)	PWEH	140	--	ns
Enable Rise/Fall Time	tER,tEF	--	25	ns
Address Set-Up Time (RS,R/W,E)	tAS	10	--	ns
Address Hole Time	tAH	20	--	ns
Data Set-Up Time	tDSW	40	--	ns
Data Delay Time	tDDR	--	190	ns
Data Hold Time	tDHR	20	--	ns

10.2 Busy flag check timing



Note : IR7, IR3 : Instruction 7th bit , 3rd bit ; AC3 : Address Counter 3rd bit.

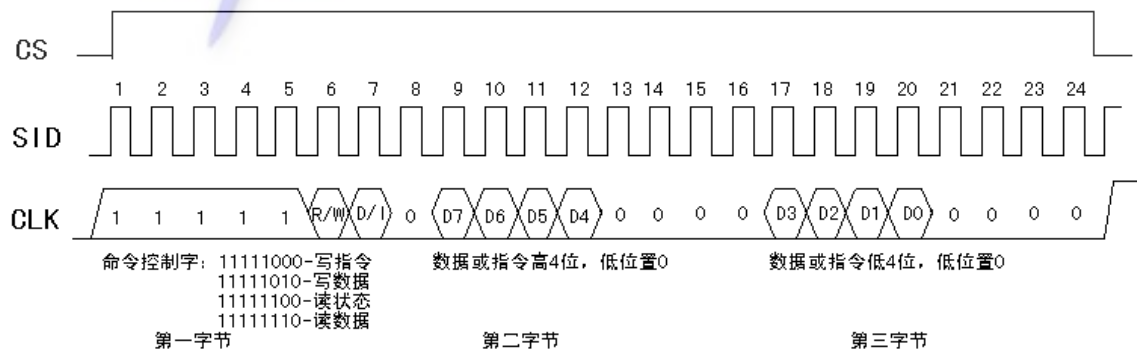
ST7920 is in serial interface mode when pull down PSB pin. Two pins (SCLK and SID) are used to complete the data transfer.

Only write data is available.

When connecting several ST7920, chip select (CS) must be used. Only when (CS) is high the serial clock (SCLK) can be accepted. On the other hand, when chip select (CS) is low ST7920 serial counter and data will be reset. Transmission will be terminated and data will be cleared. Serial transfer counter is set to the first bit. For a minimal system with only one ST7920 and one MPU, only SCLK and SID pins are necessary. CS pin should pull to high. ST7920's serial clock (SCLK) is asynchronous to the internal clock and is generated by MPU. When multiple instruction/data is transferred instruction execution time must be considered. Must wait for the previous instruction to finish before sending the next. ST7920 has no internal instruction buffer area.

When starting a transmission a start byte is required. It consists of 5 consecutive "1" (sync character). Serial transfer counter will be reset and synchronized. Following 2 bits for read/write (RW) and register/data select (RS). Last 4 bits is filled by "0". After receiving the sync character and RW and RS bits, every 8 bits instruction/data will be separated into 2 groups. Higher 4 bits (DB7~DB4) will be placed in first section followed by 4 "0". And lower 4 bits (DB3~DB0) will be placed in second section followed by 4 "0".

MPU write data:

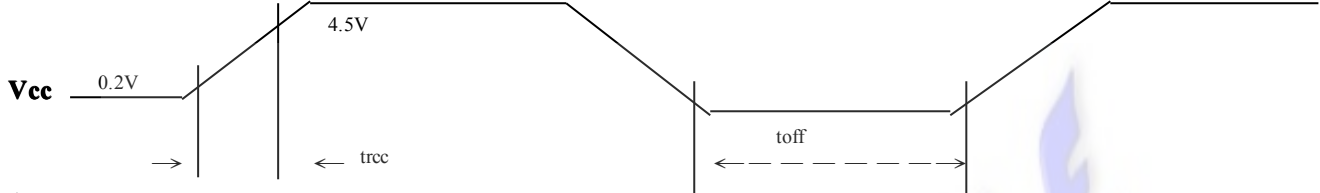


ACM12832HZ1 串口读写时序图

11. Initialization of LCM

The LCM automatically initializes (reset) when power is turned on using the internal reset circuit. If the power supply conditions for correctly operating of the internal reset circuit are not met, initialization by instruction is required. Use the procedure is next page for initialization.

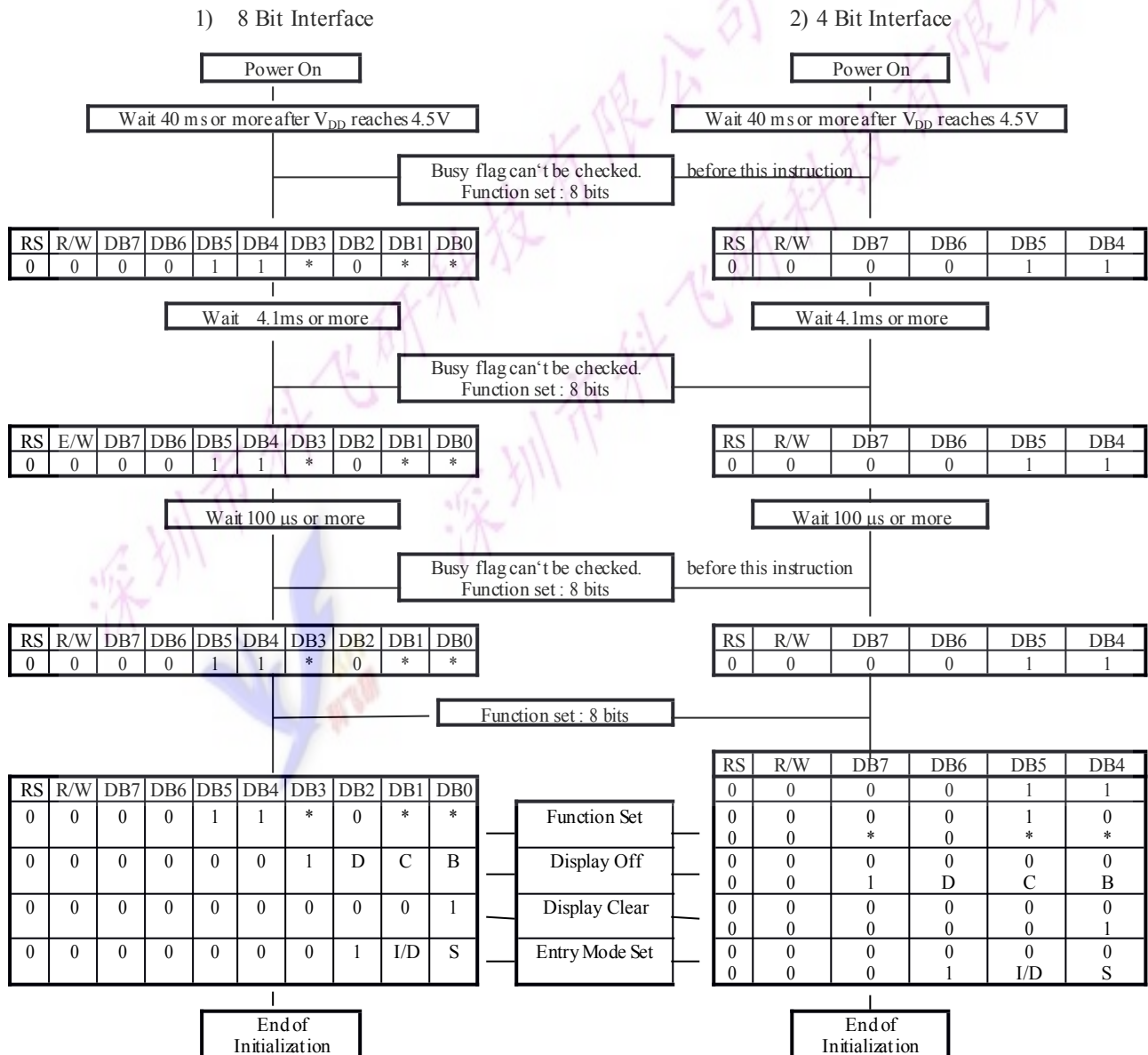
Internal Power Supply reset



(Note 1) $10\text{ ms} \geq trcc \geq 0.1\text{ ms}$, $toff \geq 1\text{ ms}$.

(Note 2) $toff$ stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

Item	Symbol	Test condition	Limit (Min.)	Limit (Max.)	Unit
Power supply rise time	$trcc$	--	0.1	10	ms
Power supply off time	$toff$	--	1	--	ms



- Busy flag is checked after instructions are completed. If busy flag isn't checked, the waiting time between instructions should be longer than execution time of these instructions.

12. Instruction Set

Instruction Table: (RE=0: Enable basic instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and return the cursor to home position (address 0).	4.6ms
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to the home position. Also returns the display being shifted to the original position. DDRAM contents remain unchanged.	4.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operation are performed during data rite/read. For normal operation. I/D=1 : increment ; 0 :decrement ; S=1 : accompanies display shift when data is written, for normal operation, set to zero.	72 μ s
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	D=1: ON display ; 0:OFF display. C=1: ON cursor ; 0: OFF cursor. B=1: ON blink cursor ; 0: OFF blink cursor.	72 μ s
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C=1: Display shift; 0:Cursor move. R/L=1: shift to right; 0: shift to left.	72 μ s
Function Set (Modify)	0	0	0	0	1	DL	X	0	X	X	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=0: Normal instruction .1: Extended instruction.	72 μ s
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	72 μ s
Set DDRAM address	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	72 μ s
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μ s
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μ s
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μ s

Instruction Table (RE=1: Enable extension instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby Mode	0	0	0	0	0	0	0	0	0	1	Enter standby mode, only Icon areas display Standby mode can be released by any other instructions.	72 μ s
Start Row Enable	0	0	0	0	0	0	0	0	1	SR	SR=1: Allow change start display Row. SR=0: Disable start display Row change.	72 μ s
Reverse Line select	0	0	0	0	0	0	0	1	R1	R0	Choice one of 4 line which data is reverse display.	72 μ s
Sleep mode and set GRAM page	0	0	0	0	0	0	1	SL	X	X	SL=0:Enter sleep mode. 1:Wake-up from sleep mode	72 μ s
Function Set (Modify)	0	0	0	0	1	DL	X	1	G	0	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=1: Extended instruction.0: Normal instruction. G=1: Graphic display ON. 0: Graphic display OFF	72 μ s
Set Iram/Start Row address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5 – AC0 is start Row. SR=0: AC5 – AC0 is ICON RAM address.	72 μ s
Set Graphic RAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set GDRAM address counter. Execute once set the address of display row (AC6-AC3). Execute again set the address of display column (AC3-AC0).	72 μ s
				0	0	0	AC3	AC2	AC1	AC0		

13. User Font Patterns (CG RAM Character)

Character Code (DDR4M data)					CGRAM Address						CGRAM data (High byte)								CGRAM data (Low byte)											
B15 – B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0				
0	X	00	X	00	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0				
					0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0		
					0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0		
					0	0	1	1	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0		
					0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0		
					0	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0		
					0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0		
					0	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	
					1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0		
					1	0	0	1	0	1	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	
					1	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0		
					1	0	1	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
					1	1	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	0	
					1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
					0	X	01	X	01	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	0						0	1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0		
0	0	1	0	0						0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
0	0	1	1	1						1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
0	1	0	0	0						1	0	1	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	
0	1	0	1	0						1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0		
0	1	1	0	0						0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	
0	1	1	1	1						1	1	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0		
1	0	0	0	0						0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	
1	0	0	1	0						0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	
1	0	1	0	0						0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
1	0	1	1	1						1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
1	1	0	0	0						0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
1	1	0	1	0						0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	0						0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	

14. Icon RAM Data

Icon RAM Address				Icon RAM Data															
				High Byte								Low Byte							
AC3	AC2	AC1	AC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Seg0	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	Seg8	Seg9	Seg10	Seg11	Seg12	Seg13	Seg14	Seg15
0	0	0	1	Seg16	Seg17	Seg18	Seg19	Seg20	Seg21	Seg22	Seg23	Seg24	Seg25	Seg26	Seg27	Seg28	Seg29	Seg30	Seg31
0	0	1	0	Seg32	Seg33	Seg34	Seg35	Seg36	Seg37	Seg38	Seg39	Seg40	Seg41	Seg42	Seg43	Seg44	Seg45	Seg46	Seg47
0	0	1	1	Seg48	Seg49	Seg50	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63
0	1	0	0	Seg64	Seg65	Seg66	Seg67	Seg68	Seg69	Seg70	Seg71	Seg72	Seg73	Seg74	Seg75	Seg76	Seg77	Seg78	Seg79
0	1	0	1	Seg80	Seg81	Seg82	Seg83	Seg84	Seg85	Seg86	Seg87	Seg88	Seg89	Seg90	Seg91	Seg92	Seg93	Seg94	Seg95
0	1	1	0	Seg96	Seg97	Seg98	Seg99	Seg100	Seg101	Seg102	Seg103	Seg104	Seg105	Seg106	Seg107	Seg108	Seg109	Seg110	Seg111
0	1	1	1	Seg112	Seg113	Seg114	Seg115	Seg116	Seg117	Seg118	Seg119	Seg120	Seg121	Seg122	Seg123	Seg124	Seg125	Seg126	Seg127
1	0	0	0	Seg128	Seg129	Seg130	Seg131	Seg132	Seg133	Seg134	Seg135	Seg136	Seg137	Seg138	Seg139	Seg140	Seg141	Seg142	Seg143
1	0	0	1	Seg144	Seg145	Seg146	Seg147	Seg148	Seg149	Seg150	Seg151	Seg152	Seg153	Seg154	Seg155	Seg156	Seg157	Seg158	Seg159
1	0	1	0	Seg160	Seg161	Seg162	Seg163	Seg164	Seg165	Seg166	Seg167	Seg168	Seg169	Seg170	Seg171	Seg172	Seg173	Seg174	Seg175
1	0	1	1	Seg176	Seg177	Seg178	Seg179	Seg180	Seg181	Seg182	Seg183	Seg184	Seg185	Seg186	Seg187	Seg188	Seg189	Seg190	Seg191
1	1	0	0	Seg192	Seg193	Seg194	Seg195	Seg196	Seg197	Seg198	Seg199	Seg200	Seg201	Seg202	Seg203	Seg204	Seg205	Seg206	Seg207
1	1	0	1	Seg208	Seg209	Seg210	Seg211	Seg212	Seg213	Seg214	Seg215	Seg216	Seg217	Seg218	Seg219	Seg220	Seg221	Seg222	Seg223
1	1	1	0	Seg224	Seg225	Seg226	Seg227	Seg228	Seg229	Seg230	Seg231	Seg232	Seg233	Seg234	Seg235	Seg236	Seg237	Seg238	Seg239
1	1	1	1	Seg240	Seg241	Seg242	Seg243	Seg244	Seg245	Seg246	Seg247	Seg248	Seg249	Seg250	Seg251	Seg252	Seg253	Seg254	Seg255

15. Graph Display RAM Address

GDRAM Column Address	GDRAM Row Address			
	0	1	—	15
0	D15 → D0	D15 → D0	D15 → D0	D15 → D0
1	D15 → D0	D15 → D0	D15 → D0	D15 → D0
2	D15 → D0	D15 → D0	D15 → D0	D15 → D0
:	:	:	:	:
61	D15 → D0	D15 → D0	D15 → D0	D15 → D0
62	D15 → D0	D15 → D0	D15 → D0	D15 → D0
63	D15 → D0	D15 → D0	D15 → D0	D15 → D0

16. Software Example

16.1 8-bit operation (8 bits 2 lines)

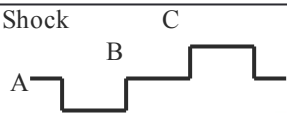
Function	R S	R W	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	Display	Description
Power on delay												Initialization. No display appears.
Function set	0	0	0	0	1	1	0	0	0	x		Sets to 8-bit operation and selects 2-line display character font. (Note: number of display lines and character fonts cannot be change after this.)
Display OFF	0	0	0	0	0	0	1	0	0	0		Turn off display.
Display ON	0	0	0	0	0	0	1	1	1	0	—	Turn on display and cursor
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	—	Set mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM Display is not shifted.
Write data to CG/DD RAM	1	0	1	0	1	1	0	1	1	0	雄	Write “雄”. Cursor incremented by one and shift to right.
Write data to CG/DD RAM	1	0	1	1	0	0	0	1	0	1	雄	Write “雄”.
Set DD RAM	0	0	1	0	1	0	0	0	0	0	雄	Set RAM address so that the cursor is propositioned at the head of the second line.
Write data to CG/DD RAM			*								雄	Write “C”, and “R”.
Cursor or display shift	0	0	0	0	0	1	0	0	x	x	雄	Shift only the cursor position to the left.
Write data to CG/DD RAM			*								雄	Write “O., LTD.”.
Entry Mode Set	0	0	0	0	0	0	0	1	1	1	雄	Set display mode shift at the time during writing operation.
Write data to CG/DD RAM	1	0	0	1	1	1	1	0	0	0	雄	Write “ x”. Cursor incremented by one and shift to right. (The display move to left.)
Write data to CG/DD RAM			*									Write other characters.
Return Home	0	0	0	0	0	0	0	0	1	0	雄	Return both display and cursor to the original position (Set address to zero).

16.2 4-bit operation (4-bit, 1 line)

Function	RS	R/ W	D7	D6	D5	D4	Display	Description
power on delay								initialization. No display appears.
Function set	0	0	0	0	1	0		Sets to 4-bit operation. In this case, operation is handled as 8-bits by initialization, and only this instruction completes with one write.
Function set	0	0	0	0	1	0		Sets 4-bit operation and selects 1-line display character font on and resetting is needed. (number of display lines and character fonts cannot be changed hence after).
Display ON/OFF Control	0	0	0	0	0	0	—	Turn on display and cursor.
Entry Mode Set	0	0	0	0	0	0	—	Set mode to incremented the address by one and to shift the cursor to the right, at the time of write. to the DD/CG RAM display is not shifted.
Write data to CG/DD RAM	1	0	1	0	1	1	雄	Write “雄”. Cursor incremented by one and shift to right.
	1	0	0	1	1	0		
	1	0	1	0	1	0		
	1	0	1	1	1	1		

same as 8-bit operation

17. Reliability Condition

		TN Type		STN Type	
		Normal Temp.	Wide Temp.	Normal Temp.	Wide Temp.
Viewing Angle	Horizontal Φ	$\pm 30^{\circ}$	$\pm 30^{\circ}$	$\pm 30^{\circ}$	$\pm 30^{\circ}$
	Vertical Θ (mm)	10° to 30°	10° to 30°	-10° to 40°	-10° to 40°
Operating Temperature		-10 to 70°C	-25 to 80°C	0 to 50°C	*-20 to 70°C
Storage Temperature		-20 to 80°C	-35 to 90°C	-20 to 70°C	*-30 to 80°C
High Temperature (Power Off)		240 Hours @ 70°C	240 Hours @ 90°C	240 Hours @ 65°C	240 Hours @ 75°C
Low Temperature (Power Off)		240 Hours @- 20°C	240 Hours @- 35°C	240 Hours @- 15°C	240 Hours @- 25°C
High Temperature (Power On)		240 Hours @ 70°C	240 Hours @ 80°C	240 Hours @ 60°C	240 Hours @ 70°C
Low Temperature (Power On)		240 Hours @- 10°C	240 Hours @- 25°C	240 Hours @- 10°C	240 Hours @- 20°C
High Temperature & High Humidity		$55^{\circ}\text{C}/90\%\text{RH}$ 240 Hours	$75^{\circ}\text{C}/90\%\text{RH}$ 240 Hours	$45^{\circ}\text{C}/90\%\text{RH}$ 240 Hours	$65^{\circ}\text{C}/90\%\text{RH}$ 240 Hours
Thermal Shock 5 Cycle		A	60min@- 20°C	60min@- 35°C	60min@- 20°C
		B	5min@ 25°C	5min@ 25°C	5min@ 25°C
		C	60min@ 70°C	60min@ 90°C	60min@ 70°C
Expected Lift		50,000 Hours	50,000 Hours	50,000 Hours	50,000 Hours

*Wide temp. version may not available for some products, Please consult our sales engineer or representative.

18. Functional Test & Inspection Criteria

18.1 Sample plan

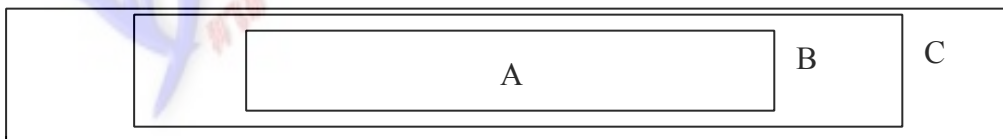
Sample plan according to MIL-STD-105D level 2, and acceptance/rejection criteria is.

Base on : Major defect : AQL 0.65 Minor defect : AQL 2.5

18.2 Inspection condition

Viewing distance for cosmetic inspection is 30cm with bare eyes, and under an environment of 800 lus (20W) light intensity. All direction for inspecting the sample should be within 45° against perpendicular line.

18.3 Definition of Inspection Zone in LCD



Zone A : Character / Digit area

Zone B : Viewing area except Zone A (Zone A + Zone B = minimum Viewing area)

Zone C : Outside viewing area (invisible area after assembly in customer's product)

Note : As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

18.4 Major Defect

All functional defects such as open (or missing segment), short, contrast differential, excess power consumption, smearing, leakage, etc. and overall outline dimension beyond the drawing. Are classified as major defects.

18.5 Minor Defect

Except the Major defects above, all cosmetic defects are classified as minor defects.

Item No.	Item to be Inspected	Inspection Standard				Classification of defects
1.	Spot defect (Defects in spot from)	Zone size (mm)	Acceptable Qty			Minor
			A	B	C	
		$\Phi \leq 0.15$	Acceptable (clutering of spot not allowed)		Acceptable	
		$0.15 \leq \Phi \leq 0.20$	1	2		
		$0.20 \leq \Phi \leq 0.25$	0	1		
		$\Phi > 0.25$	0	0		
		Remarks : for dark/white spot, size Φ is defined as $\Phi = 1/2(X+Y)$				
2.	Line defect (Defects in line form)	Size (mm)		Acceptable Qty		Minor
		L Length	W Width	Zone		
		Acceptable	$W \leq 0.02$	Acceptable	Acceptable	
		$L \leq 3.0$	$W \leq 0.03$	2		
		$L > 2.5$	$W \leq 0.03$	0		
		$L \leq 3.0$	$0.03 < W \leq 0.05$	2		
		$L > 2.5$	$0.03 < W \leq 0.05$	0		
			$W > 0.05$	Counted as spot defect (Follows item 18.5.1)		
		Remarks: The total of spot defect and line defect shall not exceed four.				
3.	Orientation defect (such as misalignment of L/C)	Not allowed inside viewing area (Zone A or Zone B)				Minor
4.	Polarizing	18.5.4.1 Polarizer Position 1. Shifting in Position Should not exceed the glass outline dimension. 2. Incomplete covering of the viewing area due to Shifting is not allowed.				Minor
		18.5.4.2 Seratches, bubble or dent on Glass/ Polarizer/ Reflector, Bubble between Polarizer & Reflector/Glass:				
		Size (mm)	Acceptable Qty			
			Zone			
			A	B	C	
		$\Phi \leq 0.20$	Acceptable		Acceptable	
		$0.20 < \Phi \leq 0.50$	3			
		$0.50 < \Phi \leq 1.00$	2			
		$\Phi > 1.00$	0			

19. Character Generator ROM Map

	Low 4-bit															
High 4-bit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1	►	◄	↑	!!	¶	§	■	↓	↑	↓	→	←	L	↔	▲	▼
2		!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	'	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	△

字型碼，前 127碼為標準 ASCII 碼，在中文為半形，中文碼由 A140 開始，共 8000 字，編碼方式為 BIG-5 碼。

**Write data from A into INSTRUCTION Register
WRINS:**

RS EQU P3.3
RW EQU P3.4
E EQU P3.5
PSB EQU P3.0
RST EQU P3.6

COM EQU 20H
DAT EQU 21H
X EQU 30H
Y EQU 31H
Z EQU 32H
SC EQU 33H
W EQU 34H

ORG 0000H
MOV SP,#60H
LJMP DISP
ORG 0040H

DISP: CLR PSB
LCALL DELAY
SETB PSB

LCALL DELAY
MOV COM,#30H ;功能设置
ACALL WRI ;写指令

LCALL DELAY ;延迟 39uS

MOV COM,#0CH ;显示开/关控制
ACALL WRI ;写指令

LCALL DELAY ;延迟 39uS

MOV COM,#01H ;清屏
ACALL WRI ;写指令

LCALL DELAY ;延迟 39uS

MOV COM,#06H ;输入方式设置
ACALL WRI ;写指令

AGAIN:
MOV COM,#01H ;清屏

ACALL WRI ;写指令

LCALL DEF_CHAR

MOV COM,#80H

LCALL WRI

MOV COM,#01H ;清屏

LCALL WRI ;写指令

MOV COM,#80H

LCALL WRI

MOV R3,#8

TEST11:MOV DPTR,#CGRAM1 ;CGRAM TEST ;隔行

LCALL WRITE_CGRAM

DJNZ R3,TEST11

MOV COM,#90H

LCALL WRI

MOV R3,#8

TEST12:

MOV DPTR,#CGRAM1

LCALL WRITE_CGRAM

DJNZ R3,TEST12

LCALL DELAY1

JB P3.7,\$

MOV COM,#01H ;清屏

ACALL WRI ;写指令

MOV COM,#80H ;隔列

LCALL WRI

MOV R3,#8

TEST21:MOV DPTR,#CGRAM2

LCALL WRITE_CGRAM

DJNZ R3,TEST21

MOV COM,#90H

LCALL WRI

MOV R3,#8

TEST22:MOV DPTR,#CGRAM2

```
LCALL WRITE_CGRAM
DJNZ R3,TEST22
LCALL DELAY1
JB P3.7,$
```

```
MOV COM,#80H ;全黑
```

```
LCALL WRI
```

```
MOV R3,#8
```

```
TEST31:MOV DPTR,#CGRAM3
```

```
LCALL WRITE_CGRAM
```

```
DJNZ R3,TEST31
```

```
MOV COM,#90H
```

```
LCALL WRI
```

```
MOV R3,#8
```

```
TEST32:MOV DPTR,#CGRAM3
```

```
LCALL WRITE_CGRAM
```

```
DJNZ R3,TEST32
```

```
LCALL DELAY1
```

```
JB P3.7,$
```

***** ;全白

```
MOV COM,#01H ;清屏
```

```
LCALL WRI ;写指令
```

```
LCALL DELAY1
```

```
JB P3.7,$
```

***** ;雪花

```
MOV COM,#80H
```

```
LCALL WRI
```

```
MOV R3,#8
```

```
TEST41:MOV DPTR,#CGRAM4
```

```
LCALL WRITE_CGRAM
```

```
DJNZ R3,TEST41
```

```
MOV COM,#90H
```

```
LCALL WRI
```

```
MOV R3,#8
```

```
TEST42:MOV DPTR,#CGRAM4
```

```
LCALL WRITE_CGRAM
```

```
DJNZ R3,TEST42
```

LCALL DELAY1

JB P3.7,\$

*****;显示月

NEXT1: MOV R4,#15 ;递增 16 次
MOV COM,#80H ;设置 DDRAM 的地址/第一行的起始地址
ACALL WRI
DEMO10: MOV A,#048H
MOV DAT,A
LCALL WRD ;写显示数据
DJNZ R4,DEMO10 ;循环 24 次，不够 16 次跳到 DEMO1 继续执行
MOV A,#00H
MOV DAT,A
LCALL WRD ;写显示数据

MOV R4,#15
MOV COM,#090H ;设置 DDRAM 的地址/第二行的起始地址
ACALL WRI
DEMO20: MOV A,#048H
MOV DAT,A
LCALL WRD ;写显示数据
DJNZ R4,DEMO20 ;循环 16 次，不够 16 次跳到 DEMO4 继续执行
MOV A,#00H
MOV DAT,A
LCALL WRD ;写显示数据

LCALL DELAY1

JB P3.7,\$

MOV COM,#01H ;清屏
ACALL WRI ;写指令

LJMP AGAIN

DEF_CHAR: ;WRITE TO CGRAM
MOV COM,#01000000B ;SET CGRAM ADDRESS
LCALL WRI
MOV R3,#8

DEF1:MOV DAT,#000H
LCALL WRD
LCALL WRD

MOV DAT,#0FFH
LCALL WRD
LCALL WRD

DJNZ R3,DEF1
MOV R3,#8

DEF2:MOV DAT,#0AAH
LCALL WRD
LCALL WRD

MOV DAT,#0AAH
LCALL WRD
LCALL WRD
DJNZ R3,DEF2
MOV R3,#8

DEF3:MOV DAT,#0FFH
LCALL WRD
LCALL WRD

MOV DAT,#0FFH
LCALL WRD
LCALL WRD
DJNZ R3,DEF3

MOV R3,#8

DEF4:MOV DAT,#0AAH
LCALL WRD
LCALL WRD

MOV DAT,#055H
LCALL WRD
LCALL WRD

DJNZ R3,DEF4
MOV R3,#8
RET

WRITE_CGRAM: ;CGRAM TESTING

CLR A
MOVC A,@A+DPTR
MOV DAT,A
LCALL WRD

INC DPTR
CLR A
MOVC A,@A+DPTR
MOV DAT,A
LCALL WRD

RET

WRI: PUSH ACC
 CLR RS
 SETB RW
WRI1: MOV P1,#0FFH
 SETB E
 MOV A,P1
 CLR E
 JB ACC.7,WRI1
 CLR RW
 MOV P1,COM
 SETB E
 CLR E
 POP ACC
 RET

WRD: PUSH ACC
 CLR RS
 SETB RW
WRD1: MOV P1,#0FFH
 SETB E
 MOV A,P1
 CLR E
 JB ACC.7,WRD1
 SETB RS
 CLR RW
 MOV P1,DAT
 SETB E

CLR E
POP ACC
RET

GDRAMADD:

MOV COM,Y
LCALL WRI

MOV COM,X
LCALL WRI
RET

SCROLL:

MOV COM,SC
LCALL WRI
RET

DELAY: MOV R7,#0FFH ;06D

DELAY4: MOV R6,#00FH ;07D

LOOP2: DJNZ R6,LOOP2
DJNZ R7,DELAY4
RET

DELAY1: MOV R4,#08

DELAY11: MOV R7,#0FFH ;06D

DELAY41: MOV R6,#0FFH ;07D

DJNZ R6,\$
DJNZ R7,DELAY41
DJNZ R4,DELAY11
RET

XX: MOV R5,#0FFH

XX1: MOV R6,#0FFH

XX2: DJNZ R6,XX2
DJNZ R5,XX1
RET

CGRAM1: DB 000H,000H ;这里是自造字符地址表

CGRAM2: DB 000H,002H

CGRAM3: DB 000H,004H

CGRAM4: DB 000H,006H

END

Write data from A into DATA Register

WRDATA:

;LCM 接口:1:GND 2:VCC 3:V0 4.SCLK(E) 5:SID(RW) 6:CS(RS)

CS EQU P3.5 ;RS
SID EQU P3.4 ;RW
SCLK EQU P3.3 ;E
;PSB EQU P3.0
;RST EQU P3.6

COM EQU 20H
DAT EQU 21H
X EQU 30H
Y EQU 31H
Z EQU 32H
SC EQU 33H
W EQU 34H

ORG 0000H
MOV SP,#60H
LJMP DISP
ORG 0040H

DISP:

SETB CS
SETB SID
SETB SCLK
;LCALL DELAY
MOV COM,#30H ;功能设置
ACALL WRIS ;写指令

;LCALL DELAY ;延迟 39uS

MOV COM,#0CH ;显示开/关控制
ACALL WRIS ;写指令

;LCALL DELAY ;延迟 39uS

MOV COM,#01H ;清屏
ACALL WRIS ;写指令

;LCALL DELAY ;延迟 39uS

MOV COM,#06H ;输入方式设置
ACALL WRIS ;写指令

AGAIN:

MOV COM,#01H ;清屏
ACALL WRIS ;写指令

LCALL DEF_CHAR
MOV COM,#80H
LCALL WRIS

MOV COM,#01H ;清屏
LCALL WRIS ;写指令

MOV COM,#80H
LCALL WRIS

TEST11: MOV R3,#8
MOV DPTR,#CGRAM1 ;CGRAM TEST ;隔行
LCALL WRITE_CGRAM
DJNZ R3,TEST11

MOV COM,#90H
LCALL WRIS
MOV R3,#8

TEST12:

MOV DPTR,#CGRAM1
LCALL WRITE_CGRAM
DJNZ R3,TEST12
LCALL DELAY1
JB P3.7,\$

MOV COM,#01H ;清屏
ACALL WRIS ;写指令

MOV COM,#80H ;隔列
LCALL WRIS
MOV R3,#8

TEST21: MOV DPTR,#CGRAM2
LCALL WRITE_CGRAM
DJNZ R3,TEST21

```

MOV      COM,#90H
LCALL    WRIS
MOV      R3,#8
TEST22:  MOV      DPTR,#CGRAM2
LCALL    WRITE_CGRAM
DJNZ     R3,TEST22
LCALL    DELAY1
JB       P3.7,$

```

```

MOV      COM,#80H                                ;全黑
LCALL    WRIS
MOV      R3,#8
TEST31:  MOV      DPTR,#CGRAM3
LCALL    WRITE_CGRAM
DJNZ     R3,TEST31

```

```

MOV      COM,#90H
LCALL    WRIS
MOV      R3,#8
TEST32:  MOV      DPTR,#CGRAM3
LCALL    WRITE_CGRAM
DJNZ     R3,TEST32
LCALL    DELAY1
JB       P3.7,$

```

***** ;全白

```

MOV      COM,#01H                                ;清屏
LCALL    WRIS                                    ;写指令

```

```

LCALL    DELAY1
JB       P3.7,$

```

***** ;雪花

```

MOV      COM,#80H
LCALL    WRIS
MOV      R3,#8
TEST41:  MOV      DPTR,#CGRAM4
LCALL    WRITE_CGRAM
DJNZ     R3,TEST41

```

```

MOV      COM,#90H
LCALL    WRIS

```

```

MOV      R3,#8
TEST42: MOV      DPTR,#CGRAM4
        LCALL    WRITE_CGRAM
        DJNZ     R3,TEST42
        LCALL    DELAY1
        JB       P3.7,$

        LCALL    DEF_CHAR
        MOV      COM,#80H
        LCALL    WRIS

        MOV      COM,#01H          ;清屏
        LCALL    WRIS              ;写指令
;*****;显示月
NEXT1:   MOV      R4,#15           ;递增 16 次
        MOV      COM,#80H         ;设置 DDRAM 的地址/第一行的起始地址
        LCALL    WRIS
DEMO10:  MOV      A,#048H
        MOV      DAT,A
        LCALL    WRDS              ;写显示数据
        DJNZ     R4,DEMO10        ;循环 24 次，不够 16 次跳到 DEMO1 继续执行
        MOV      A,#00H
        MOV      DAT,A
        LCALL    WRDS              ;写显示数据

        MOV      R4,#15
        MOV      COM,#090H        ;设置 DDRAM 的地址/第二行的起始地址
        LCALL    WRIS
DEMO20:  MOV      A,#048H
        MOV      DAT,A
        LCALL    WRDS              ;写显示数据
        DJNZ     R4,DEMO20        ;循环 16 次，不够 16 次跳到 DEMO4 继续执行
        MOV      A,#00H
        MOV      DAT,A
        LCALL    WRDS              ;写显示数据

        LCALL    DELAY1
        JB       P3.7,$

        MOV      COM,#01H          ;清屏
        ACALL    WRIS              ;写指令

```

LJMP AGAIN

DEF_CHAR: ;WRITE TO CGRAM
 MOV COM,#01000000B ;SET CGRAM ADDRESS
 LCALL WRIS
 MOV R3,#8

DEF1: MOV DAT,#000H
 LCALL WRDS
 LCALL WRDS

 MOV DAT,#0FFH
 LCALL WRDS
 LCALL WRDS

 DJNZ R3,DEF1
 MOV R3,#8

DEF2: MOV DAT,#0AAH
 LCALL WRDS
 LCALL WRDS

 MOV DAT,#0AAH
 LCALL WRDS
 LCALL WRDS
 DJNZ R3,DEF2
 MOV R3,#8

DEF3: MOV DAT,#0FFH
 LCALL WRDS
 LCALL WRDS

 MOV DAT,#0FFH
 LCALL WRDS
 LCALL WRDS
 DJNZ R3,DEF3

 MOV R3,#8
DEF4: MOV DAT,#0AAH
 LCALL WRDS

LCALL WRDS

MOV DAT,#055H

LCALL WRDS

LCALL WRDS

DJNZ R3,DEF4

MOV R3,#8

RET

WRITE_CGRAM: ;CGRAM TESTING

CLR A

MOVC A,@A+DPTR

MOV DAT,A

LCALL WRDS

INC DPTR

CLR A

MOVC A,@A+DPTR

MOV DAT,A

LCALL WRDS

RET

WRIS: PUSH ACC

SETB CS

SETB SID ;从 SID 送出五个"1"到 7920 的指令寄存器

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

CLR SID ;分别从 SID 送出 RW,RS,0 到 7920 的指令寄存器

SETB SCLK
CLR SCLK

SETB SCLK
CLR SCLK

SETB SCLK
CLR SCLK

MOV A,COM ;送出指令到 7920 指令寄存器

RLC A

MOV SID,C

SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

CLR SID ;用"0"补足低四位:D3,D2,D1,D0

SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK

LCALL DELAY
;LCALL DELAY

RLC A
MOV SID,C
SETB SCLK
CLR SCLK
RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

CLR SID ;用"0"补足低四位:D7,D6,D5,D4
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
POP ACC
RET

WRDS: PUSH ACC

SETB CS
SETB SID ;从 SID 送出五个"1"到 7920 的指令寄存器

CLR SCLK
SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

SETB SCLK

CLR SCLK

CLR SID

;分别从 SID 送出 RW,RS,0 到 7920 的指令寄存器

SETB SCLK

;RW 为 0 表示进行写操作

CLR SCLK

SETB SID

;RS 为 1 表示传输的是数据

SETB SCLK

CLR SCLK

CLR SID

SETB SCLK

CLR SCLK

MOV A,DAT

;送出数据到 7920 的数据寄存器

RLC A

MOV SID,C

;bit7---bit4

SETB SCLK

CLR SCLK

RLC A

MOV SID,C

SETB SCLK

CLR SCLK

RLC A

MOV SID,C

SETB SCLK

CLR SCLK

RLC A

MOV SID,C

SETB SCLK
CLR SCLK

CLR SID ;用"0"补足低四位:D3,D2,D1,D0

SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

RLC A
MOV SID,C
SETB SCLK
CLR SCLK

CLR SID ;用"0"补足低四位:D7,D6,D5,D4

SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK
SETB SCLK
CLR SCLK

```

        POP      ACC
        RET
GDRAMADD:
        MOV      COM,Y
        LCALL    WRIS

        MOV      COM,X
        LCALL    WRIS
        RET

```

```

DELAY:  MOV      R7,#0BFH    ;06D
DELAY4: MOV      R6,#001H    ;07D
LOOP2:  DJNZ     R6,LOOP2
        DJNZ     R7,DELAY4
        RET

```

```

DELAY1: MOV      R4,#08
DELAY11:MOV      R7,#0FFH    ;06D
DELAY41:MOV      R6,#0FFH    ;07D
        DJNZ     R6,$
        DJNZ     R7,DELAY41
        DJNZ     R4,DELAY11
        RET

```

```

XX:     MOV      R5,#0FFH
XX1:    MOV      R6,#0FFH
XX2:    DJNZ     R6,XX2
        DJNZ     R5,XX1
        RET

```

```

CGRAM1: DB 000H,000H      ;这里是自造字符地址表
CGRAM2: DB 000H,002H
CGRAM3: DB 000H,004H
CGRAM4: DB 000H,006H
        END

```


CEA0 巍 微 危 韦 违 桅 围 唯 惟 为 淮 维 苇 萎 委
CEB0 伟 伪 尾 文 蔚 味 畏 胃 魏 渭 谓 翁 尉 慰
CEC0 卫 瘟 尾 闻 纹 问 翁 尉 尉 尉 尉 尉 尉 尉
CED0 涡 瘟 我 卧 握 沃 吻 翁 翁 翁 翁 翁 翁 翁
CEE0 梧 吾 吴 武 五 沃 吻 吻 吻 吻 吻 吻 吻
CEF0 勿 务 悟 昔 熙 析 西 惜 溪 污 伍 污 污 污
CFA0 稀 息 希 膝 夕 惜 溪 溪 溪 溪 溪 溪 溪
CFB0 媳 喜 洗 膝 下 歛 歛 歛 歛 歛 歛 歛
CFC0 侠 狭 涎 显 显 显 显 显 显 显 显 显
CFD0 闲 涎 涎 显 显 显 显 显 显 显 显 显
CFE0 相 涎 涎 显 显 显 显 显 显 显 显 显
CFF0 橡 橡 橡 橡 橡 橡 橡 橡 橡 橡 橡
DOA0 小 邪 邪 邪 邪 邪 邪 邪 邪 邪 邪
DOB0 邪 邪 邪 邪 邪 邪 邪 邪 邪 邪 邪
DOC0 欣 欣 欣 欣 欣 欣 欣 欣 欣 欣 欣
DOD0 行 行 行 行 行 行 行 行 行 行 行
DOE0 朽 朽 朽 朽 朽 朽 朽 朽 朽 朽 朽
DOF0 叙 叙 叙 叙 叙 叙 叙 叙 叙 叙 叙
DIA0 选 选 选 选 选 选 选 选 选 选 选
DIB0 寻 寻 寻 寻 寻 寻 寻 寻 寻 寻 寻
DIC0 牙 牙 牙 牙 牙 牙 牙 牙 牙 牙 牙
DID0 研 研 研 研 研 研 研 研 研 研 研
DIE0 燕 燕 燕 燕 燕 燕 燕 燕 燕 燕 燕
DIF0 伴 伴 伴 伴 伴 伴 伴 伴 伴 伴 伴
D2A0 摇 摇 摇 摇 摇 摇 摇 摇 摇 摇 摇
D2B0 野 野 野 野 野 野 野 野 野 野 野
D2C0 依 依 依 依 依 依 依 依 依 依 依
D2D0 倚 倚 倚 倚 倚 倚 倚 倚 倚 倚 倚
D2E0 亦 亦 亦 亦 亦 亦 亦 亦 亦 亦 亦
D2F0 茵 茵 茵 茵 茵 茵 茵 茵 茵 茵 茵
D3A0 影 影 影 影 影 影 影 影 影 影 影
D3B0 影 影 影 影 影 影 影 影 影 影 影
D3C0 永 永 永 永 永 永 永 永 永 永 永
D3D0 有 有 有 有 有 有 有 有 有 有 有
D3E0 余 余 余 余 余 余 余 余 余 余 余
D3F0 羽 羽 羽 羽 羽 羽 羽 羽 羽 羽 羽
D4A0 园 园 园 园 园 园 园 园 园 园 园
D4B0 岳 岳 岳 岳 岳 岳 岳 岳 岳 岳 岳
D4C0 岳 岳 岳 岳 岳 岳 岳 岳 岳 岳 岳
D4D0 孕 孕 孕 孕 孕 孕 孕 孕 孕 孕 孕
D4E0 脏 脏 脏 脏 脏 脏 脏 脏 脏 脏 脏
D4F0 责 责 责 责 责 责 责 责 责 责 责
D5A0 镊 镊 镊 镊 镊 镊 镊 镊 镊 镊 镊
D5B0 瞻 瞻 瞻 瞻 瞻 瞻 瞻 瞻 瞻 瞻 瞻
D5C0 绽 绽 绽 绽 绽 绽 绽 绽 绽 绽 绽
D5D0 招 招 招 招 招 招 招 招 招 招 招
D5E0 褚 褚 褚 褚 褚 褚 褚 褚 褚 褚 褚
D5F0 震 震 震 震 震 震 震 震 震 震 震
D6A0 帧 帧 帧 帧 帧 帧 帧 帧 帧 帧 帧
D6B0 职 职 职 职 职 职 职 职 职 职 职
D6C0 掷 掷 掷 掷 掷 掷 掷 掷 掷 掷 掷
D6D0 中 中 中 中 中 中 中 中 中 中 中
D6E0 粥 粥 粥 粥 粥 粥 粥 粥 粥 粥 粥
D6F0 逐 逐 逐 逐 逐 逐 逐 逐 逐 逐 逐
D7A0 住 住 住 住 住 住 住 住 住 住 住
D7B0 装 装 装 装 装 装 装 装 装 装 装
D7C0 桌 桌 桌 桌 桌 桌 桌 桌 桌 桌 桌
D7D0 仔 仔 仔 仔 仔 仔 仔 仔 仔 仔 仔
D7E0 奏 奏 奏 奏 奏 奏 奏 奏 奏 奏 奏

D7F0 尊 遵 昨 左 佐 柞 做 作 坐 座 甬 舜 疆 一 禺 丿
D8A0 匕 于 天 兀 巧 柞 州 丕 坐 丞 甬 舜 疆 一 禺 丿
D8B0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D8C0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D8D0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D8E0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D8F0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9A0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9B0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9C0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9D0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9E0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
D9F0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAD0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DAF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DBA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DBB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DBC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DBE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DBF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DCA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DCB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DCC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DCE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DCF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DDA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
ddb0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DDC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DDD0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DDE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DDE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DEA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DEB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DEC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DED0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DEE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DEF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFD0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
DFF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EQA0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EOB0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EOC0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EOD0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EOE0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
EOF0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
E1A0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
E1B0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
E1C0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘
E1D0 乱 元 丰 彡 厄 氏 凶 厶 亘 亘 亘 亘 亘 亘 亘

F5C0	趵	趿	趿	趿	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F5D0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F5E0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F5F0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6A0		跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6B0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6C0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6D0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6E0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F6F0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7A0		跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7B0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7C0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7D0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7E0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽
F7F0	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽	跽